



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,097	03/27/2001	Stepan Sokolov	SUN1P827/P6095	2544
22434	7590	08/02/2004	EXAMINER	
BEYER WEAVER & THOMAS LLP P.O. BOX 778 BERKELEY, CA 94704-0778			ALI, SYED J	
		ART UNIT		PAPER NUMBER
		2127		
DATE MAILED: 08/02/2004				

q

Please find below and/or attached an Office communication concerning this application or proceeding.

SL

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/820,097	SOKOLOV ET AL.
	Examiner	Art Unit
	Syed J Ali	2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 27 March 2001.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-24 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 28 June 2001 and 27 March 2001 is/are: a) accepted or b) objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____.   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6-8</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____.                                   |

## **DETAILED ACTION**

1. Claims 1-24 are pending in this application.

### *Specification*

2. The cross reference related to the application cited in the specification must be updated (i.e. update the relevant status, with PTO serial numbers or patent numbers where appropriate, on page 1, lines 6-22; page 13 lines 25-28. The entire specification should be so revised).

### *Claim Rejections - 35 USC § 101*

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. **Claims 1-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

5. As per claims 1-24, the claims are drawn to software per se, which does not fall within the statutory classes recited in 35 U.S.C. 101. Independent claims 1 and 5 recite “a set of virtual machine instructions”, while independent claims 9, 12, 15, 18, 21, and 23 recite “a virtual machine instruction”. In both instances, the claimed subject matter is software, per se, failing to be tangibly embodied on any sort of physical medium (See MPEP 2106). Dependent claims 2-4, 6-8, 10-11, 13-14, 16-17, 19-20, 22, and 24 are rejected for similar reasons as their parent claims, as they fail to resolve the deficiencies noted in their respective parent claims.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 1, 3, 5, 9, 12, 15, 21, and 23-are 24 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

8. Claims 1, 5, 9, 12, 15, 21, and 23-24 contain the trademark/trade name Java Bytecode. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe the instructions and, accordingly, the identification/description is indefinite.

9. Claim 3 recites the limitation “a set of virtual machine load constant instructions” in line 1. There is insufficient antecedent basis for this limitation in the claim.

***Double Patenting***

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. **Claims 1 and 5 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 09/819,120.**

12. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference in the claims is that the present application recites that the

virtual machine instructions of claim 1 are “to load constant values on an execution stack”, and the virtual machine instructions of claim 5 are “to store constant values on an execution stack”. Since the recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the conflicting claim in order to patentably distinguish the claimed invention from the conflicting claim, the limitation does not patentably distinguish the claims of the present application from claim 1 of copending application 09/819,120.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 2-4 and 6-8 are also provisionally rejected as they fail to resolve the conflicting issues presented by their respective parent claims.

***Claim Rejections - 35 USC § 102***

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. **Claims 15 and 18 rejected under 35 U.S.C. 102(b) as being anticipated by Tyma (USPN 5,903,761).**

Art Unit: 2127

15. As per claim 15, Tyma teaches the invention as claimed, including a virtual machine instruction suitable for execution in a virtual machine to duplicate values stored in an execution stack on top of the execution stack (col. 8 lines 25-35), the virtual machine instruction representing two or more Java Bytecode executable instructions that are also suitable for duplicating values stored in the execution stack on top of the execution stack (col. 1 lines 40-50).

16. As per claim 18, Tyma teaches the invention as claimed, including a virtual machine instruction suitable for execution in a virtual machine to duplicate values stored in an execution stack on top of the execution stack (col. 8 lines 25-35), wherein the virtual machine instruction has a parameter associated with it to indicate which value stored in the execution stack should be duplicated on the top of the stack (col. 1 lines 40-50).

***Claim Rejections - 35 USC § 103***

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. **Claims 1-14 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seshadri (USPN 6,658,421) in view of Tyma.**

Art Unit: 2127

19. As per claim 1, Seshadri teaches the invention as claimed, including a set of virtual machine instructions suitable for execution in a virtual machine to load constant values on an execution stack (col. 11 lines 28-49; col. 11 line 57 - col. 12 line 5), the set of virtual machine instructions representing a number of corresponding Java Bytecode executable instructions that are also suitable for execution in the virtual machine to load constant values on an execution stack (col. 10 lines 55-58; col. 10 line 65 - col. 11 line 19; col. 11 lines 28-49), and

wherein every one of the corresponding Java Bytecode executable instructions can be represented by at least one of the virtual machine instructions in the virtual machine instruction set (col. 11 line 57 - col. 12 line 24).

20. Tyma teaches the invention as claimed, including the following limitations not shown by Seshadri:

wherein the set of the virtual machine instructions consists of a number of virtual machine instructions that is less than the number of the corresponding Java Bytecode executable instructions (col. 1 lines 40-50).

21. It would have been obvious to one of ordinary skill in the art to combine Seshadri and Tyma since the method of reducing the number of bytecode instructions taught by Tyma solves drawbacks of modern compilers, such as slowed execution time for stack push and pop operations, as well as preventing reverse compilation of developed code (Tyma, col. 1 lines 21-37).

Art Unit: 2127

22. As per claim 2, Seshadri teaches the invention as claimed, including a set of virtual machine instructions as recited in claim 1, wherein the set consists of a first, a second, and a third instruction, the first instruction suitable for pushing one byte values on the execution stack (col. 8 lines 8-29; col. 11 lines 28-49), the second instruction suitable for pushing 4 byte values on the execution stack (col. 8 lines 8-29; col. 11 lines 28-49), and the third instruction suitable for pushing 8 byte values on the execution stack (col. 8 lines 8-29; col. 11 lines 28-49).

23. As per claim 3, Seshadri teaches the invention as claimed, including a set of virtual machine load constant instructions as recited in claim 1, wherein the first instruction includes a code portion and a data portion which are both represented in a code stream in the virtual machine (col. 8 lines 8-29; col. 11 line 57 - col. 12 line 24), and wherein the second instruction includes a code portion and a data portion which are respectively represented in a code stream and in a data stream in the virtual machine (col. 8 lines 8-29; col. 11 line 57 - col. 12 line 24).

24. As per claim 4, Seshadri teaches the invention as claimed, including a set of virtual machine instructions as recited in claim 3, wherein the set is suitable to load N byte constant values on the execution stack, and wherein N is a positive integer (col. 8 lines 8-29; col. 11 lines 28-49).

Art Unit: 2127

25. As per claim 5, Seshadri teaches the invention as claimed, including a set of virtual machine instructions suitable for execution in a virtual machine to store local variables onto an execution stack (col. 11 lines 28-49; col. 11 line 57 - col. 12 line 5), the set of virtual machine instructions representing a number of corresponding Java Bytecode executable instructions that are also suitable for execution in the virtual machine to store local variables onto an execution stack (col. 10 lines 55-58; col. 10 line 65 - col. 11 line 19; col. 11 lines 28-49), and

wherein every one of the corresponding Java Bytecode executable instructions can be represented by at least one of the virtual machine instructions in the virtual machine instruction set (col. 11 line 57 - col. 12 line 24).

26. Tyma teaches the invention as claimed, including the following limitations not shown by Seshadri:

wherein the set of the virtual machine instructions consists of a number of virtual machine instructions that is less than the number of the corresponding Java Bytecode executable instructions (col. 1 lines 40-50).

27. As per claim 6, Seshadri teaches the invention as claimed, including a set of virtual machine instructions as recited in claim 5, wherein the set of virtual machine instructions consists of a first instruction and a second instruction, the first instruction being suitable for storing 4 byte local variables onto the execution stack (col. 8 lines 8-29; col. 11 lines 28-49), and the second instruction being suitable for storing 8 byte local variables onto the execution stack (col. 8 lines 8-29; col. 11 lines 28-49).

Art Unit: 2127

28. As per claim 7, Seshadri teaches the invention as claimed, including a set of virtual machine instructions as recited in claim 5, wherein the first or the second instruction includes a code portion and a data portion which are respectively represented in a code stream and in a data stream in the virtual machine (col. 8 lines 8-29; col. 11 line 57 - col. 12 line 24).

29. As per claim 8, Seshadri teaches the invention as claimed, including a set of virtual machine instructions as recited in claim 5, wherein the set of set of virtual machine instructions is suitable to store N byte local variables on the execution stack, and wherein N is a positive integer (col. 8 lines 8-29; col. 11 lines 28-49).

30. As per claim 9, Seshadri teaches the invention as claimed, including a virtual machine instruction suitable for execution in a virtual machine to load values from arrays on an execution stack (col. 11 lines 28-49; col. 11 line 57 - col. 12 line 24).

31. Tyma teaches the invention as claimed, including the following limitations not shown by Seshadri:

the virtual machine instruction representing two or more Java Bytecode executable instructions that are also suitable for loading values from arrays on the execution stack (col. 1 lines 40-50).

32. As per claim 10, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 9, wherein the arrays can be an array of 1 byte values, or an array of 2 byte values, or an array of 4 byte values, or an array of 8 byte values (col. 8 lines 8-29; col. 11 lines 28-49).

33. As per claim 11, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 9, wherein a header of an array is read to determine the type of the array (col. 8 lines 8-29; col. 11 lines 28-49).

34. As per claim 12, Seshadri teaches the invention as claimed, including a virtual machine instruction suitable for execution in a virtual machine to store values located on an execution stack into arrays (col. 11 lines 28-49; col. 11 line 57 - col. 12 line 24).

35. Tyma teaches the invention as claimed, including the following limitations not shown by Seshadri:

the virtual machine instruction representing two or more Java Bytecode executable instructions that are also suitable for storing values located on an execution stack into an array (col. 1 lines 40-50).

36. As per claim 13, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 12, wherein the arrays can be an array of 1 byte values, or an array of 2 byte values, or an array of 4 byte values, or an array of 8 byte values (col. 8 lines 8-29; col. 11 lines 28-49).

37. As per claim 14, Seshadri teaches the invention as claimed, including a virtual machine load array instruction as recited in claim 12, wherein a header of an array is read to determine the type of the array (col. 8 lines 8-29; col. 11 lines 28-49).

38. As per claim 21, Seshadri teaches the invention as claimed, including a virtual machine instruction suitable for execution in a virtual machine to return values by placing them on top of an execution stack (col. 17 line 63 - col. 18 line 58).

39. Tyma teaches the invention as claimed, including the following limitations not shown by Seshadri:

the virtual machine instruction representing two or more Java Bytecode executable instructions that are also suitable for returning values by placing them on top of the execution stack (col. 1 lines 40-50).

40. As per claim 22, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 21, wherein the values returned can be 4 byte values or 8 byte values (col. 8 lines 8-29; col. 11 lines 28-49).

41. As per claim 23, Seshadri teaches the invention as claimed, including a virtual machine instruction suitable for execution in a virtual machine to instantiate Java objects and arrays (col. 11 line 57 - col. 12 line 24; col. 13 lines 29-39; col. 13 lines 51-63).

42. Tyma teaches the invention as claimed, including the following limitations not shown by Seshadri:

the virtual machine instruction representing two or more Java Bytecode executable instructions that are also suitable for instantiation of Java objects or arrays (col. 1 lines 40-50).

43. As per claim 24, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 23, wherein the instantiation of Java objects and arrays are performed by determining the type of the object or array based on a parameter that is associated with the object or array (col. 8 lines 8-29; col. 11 lines 28-49).

44. **Claims 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tyma.**

45. As per claim 16, Tyma does not explicitly teach the invention as claimed, including a virtual machine instruction as recited in claim 15, wherein values that can be duplicated on the execution stack are not limited to values that are within first, second, and third positions from the top of the stack.

46. However, the claim language “not limited to” indicates that *any value* on the execution stack can be duplicated by the virtual machine instruction. Therefore, the duplication operations taught by Tyma are considered sufficient as they duplicate the top values on the execution stack.

Art Unit: 2127

47. As per claim 19, Tyma does not explicitly teach the invention as claimed, including a virtual machine instruction as recited in claim 18, wherein values that can be duplicated are not limited to values that are within first, second, and third positions from the top of the execution stack.

48. However, the claim language “not limited to” indicates that *any value* on the execution stack can be duplicated by the virtual machine instruction. Therefore, the duplication operations taught by Tyma are considered sufficient as they duplicate the top values on the execution stack.

49. **Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tyma in view of Seshadri.**

50. As per claim 17, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 15, wherein the values duplicated on top of the stack can be 4 byte values or 8 byte values (col. 8 lines 8-29; col. 11 lines 28-49).

51. It would have been obvious to one of ordinary skill in the art to combine Tyma and Seshadri since the method of reducing the number of bytecode instructions taught by Tyma solves drawbacks of modern compilers, such as slowed execution time for stack push and pop operations, as well as preventing reverse compilation of developed code (Tyma, col. 1 lines 21-37).

Art Unit: 2127

52. As per claim 20, Seshadri teaches the invention as claimed, including a virtual machine instruction as recited in claim 18, wherein the values can be 4 byte values or 8 byte values (col. 8 lines 8-29; col. 11 lines 28-49).

### ***Conclusion***

53. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Guillen et al. (USPN 5,838,980) teaches the enhancement of virtual machine instructions before compilation to improve performance.

Morgan et al. (USPN 5,893,084) teaches an n-bit virtual machine that supports variable length instructions

Wahbe (USPN 6,151,618) teaches the safe execution of a virtual machine via generation of reduced bytecode instructions for compact execution.

Muthukaruppan (USPN 6,182,202) teaches variable length instructions including an offset that defines the length of the instruction.

Loen (USPN 6,434,625) teaches the automatic adaptation of a virtual machine in response to varying length words and byte orderings.

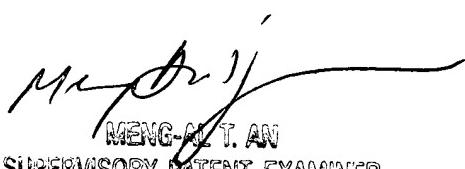
Griesemer (USPN 6,467,037) teaches the automatic alignment of bytecode instructions for fast loading and execution.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali  
July 14, 2001



MENG-AI T. AN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100